Techniques of cryogenic reactive ion etching in silicon for fabrication of sensors

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Cryogenic etching of silicon, using an inductively coupled plasma reactive ion etcher (ICP-RIE), has extraordinary properties which can lead to unique structures difficult to achieve using other etching methods. In this work, the authors demonstrate the application of ICP-RIE techniques which capitalize on the cryogenic properties to create different sensors geometries: optical, electrical, magnetic, and mechanical. The three techniques demonstrated are (1) single step deep etches with controllable sidewall profiles. Demonstrating this, silicon pillars with over 70 μm depth and less than 250 nm sidewall roughness were etched using only 1.6 μm of photoresist for use as solar cells. (2) Using the cryogenic etch for thick metallization and liftoff with a thin photoresist mask. Demonstrating this second technique, a magnetic shim was created by deposition of 6.5 μm of iron into 20 μm deep etched trenches, using the remaining 1.5 μm photoresist etch mask as the liftoff mask. Using the same technique, 15 μm of copper was lifted off leaving a 20 μm deep plasma enhanced chemical vapor deposition silicon oxide coated, silicon channel with copper. (3) Use of a two step cryogenic etch for deep etching with reduced sidewall undercutting. This was demonstrated by fabrication of deep and anisotropic microelectromechanical systems structures; a mechanical resonator was etched 183 μm deep into silicon with less than 3 μm of undercutting. This work also describes the etch parameters and etch controls for each of these sensors. [DOI: 10.1116/1.3196790]

I. INTRODUCTION

Cryogenic inductively coupled plasma reactive ion etching (ICP-RIE) of silicon has significant advantages over that of other silicon etches such as chopping Bosch or Cl_2 chemistries. In cryogenic etching, the silicon sample is cooled down to subzero temperatures, typically −100 to −140 °C.[1] These low temperatures not only enable profile control by virtue of condensation of a SiO_xF_y passivation layer but also provide extremely high etch selectivities of the etch mask over silicon. It is understood that the silicon etch product from the SF_6 etch chemistry, SiF_x, condenses on the sidewalls and combines with the reactive oxygen to create the SiO_xF_y passivation layer.[2–4] This condensate offers sidewall protection from the SF_6 chemical attack, similar to the role C_4F_8 plays in Bosch etching. Anisotropic silicon etching can thus be realized, resulting in geometries in which the verticality of the sidewalls is tightly controlled by the passivation rate. Although the etch rate and the passivation rate equations are coupled, various mechanisms for controlling the passivation rate are also separable from the etching rate equation, such as silicon surface temperature and oxygen concentration in the etching plasma. Since the passivation is occurring simultaneously with the etching, sidewall roughness introduced by scalloping, usually seen with chopping etch-passivation chemistries such as Bosch, can be eliminated yielding very smooth sidewalls with sub-250 nm roughness. The very low temperature ensures preferential etching of silicon to that of the photoresist or silicon dioxide etch mask due to the low Arrhenius activation energy for silicon. Selectivity ratios of better than 70:1 for photoresist and 150:1 for silicon dioxide have been achieved. These two advantages allow for unique structures to be fabricated in silicon.

Here, we demonstrate devices of micron sized structures using cryogenic etching recipes developed within an inductively coupled plasma system. We also detail exact etching conditions along with general trends of pattern transfer parameters for quickly reproducing this work. The device applications of the pillars described below are microfabricated radial pillar solar cells. The applications of the exceptionally thick liftoff layers of copper and iron coils embedded in silicon enable thick metal liftoff with thin photoresist layers enable the definition magnetic shims and electromagnetic coils. Finally, very deep anisotropic silicon etches described here have been optimized for the creation of microelectromechanical system (MEM) silicon mechanical resonators.

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TABLE I. Etch parameters for 5, 10, 20, and 50 μm diameter pillars in silicon.

Etch parameter	Units	Value	Etch parameter	Units	Value
SF_6	(SCCM)	70	ICP	(Watts)	900
O_2	(SCCM)	4.5	RIE	(Watts)	5
Temperature	(Celsius)	−120	Pressure	(milliTorr)	10
E_o	(μm/min)	1.15	Helium	(Torr)	10

II. SMOOTH ETCH SIDEWALLS AND ANGLE CONTROL: PILLAR ARRAYS

The first example devices presented here are silicon pillars used for characterizing silicon solar cells.[5,6] The pillars were lithographically defined in hexagonal arrays with pillar separations equal to their diameter. Sets of 5, 10, 20, and 50 μm diameter pillars were all etched in 1 mm square arrays on the same silicon sample allowing aspect ratio dependencies to become apparent. The fabrication sequence begins with cleaning a *P*-type, 1–10 Ω cm, ⟨100⟩ silicon piece, spinning AZ5214e photoresist, exposing and developing the pattern into the ~1.6 μm thick photoresist. The silicon sample, roughly 1 in.^{2}, is then mounted to a 150 mm carrier silicon wafer using a thin film of Fomblin oil. This results in excellent thermal conductivity between the sample piece and the carrier wafer, with the oil easily removed later using isopropyl alcohol. Before etching, the chamber was cleaned using a high pressure SF_6 plasma, then conditioned on a blank wafer using the etch recipe for 30 min. We find that the conditioning step is exceedingly important for obtaining reproducible results.

The sample was then cryogenically etched in an Oxford Instruments PlasmaLab System 100 ICP-RIE 380. The samples were etched under the following typical conditions (Table I).

This process, running for 40 min, resulted in 5 μm diameter pillars approximately 35 μm tall. Increasing the etch time to 80 min for the 5 μm diameter pillars results in an etch height of 76 μm, Fig. 1. Surface defects from the etch were typically less than 250 nm with occasional 600 nm defects spaced greater than 5 μm apart. This is significantly smoother than the regular pattern of chopping marks, approximately 2 μm, created using Bosch etching. Aspect ratios of over 17.5 were achieved, defined here as the ratio of etched depth to width between pillars. Since the different sized pillar arrays were created on the same substrate, it allowed for characterization of aspect ratio etching rate dependence, Fig. 2. The divergence of the etch depths between the different diameter pillars, in Fig. 2, clearly indicates that aspect ratio dependent etching is occurring.

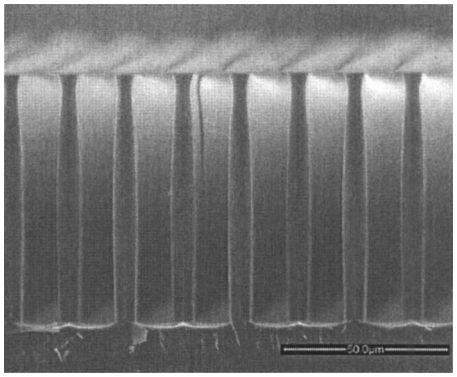

FIG. 1. Cross sectional SEM of 76 μm high, 5 μm diameter silicon pillars cryogenically etched with 4.5 SCCM of O_2. 800 nm of photoresist remained after the etch for a selectivity of 89:1 and an etch rate of 0.96 μm/min.

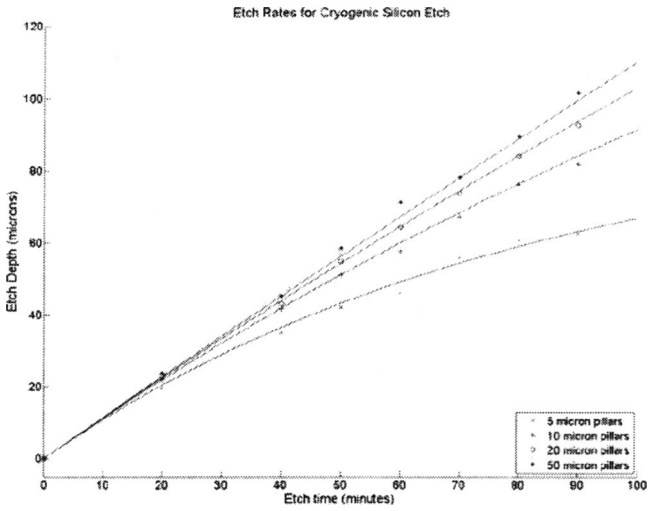

FIG. 2. Etch depth dependence on time for cryogenically etched silicon pillars. The curves generated are from the solutions to the generalized etching rate equation with the *E* coefficient set to 1.15 μm/min and *b* coefficient set to 0.040 99.

More than four contributors to aspect ratio dependent etching have been suggested.[7] The most likely candidates are Knudsen transport of neutrals, ion shadowing, neutral shadowing, and differential insulating charging. Keil and Anderson[8] correctly assessed that differentiation and measurement between the contributors in standard etchers are difficult and as a substitute rate equations may be used to describe their effects. To characterize this effect here, a differential equation for the etch rate was established similar to their Eq. 4,

$$\frac{dD}{dt} = E - b * \frac{D}{W}. \tag{1}$$

For Eq. (1), *D* is the etch depth, *E* is the etch rate for an aspect ratio of zero, *b* is a coefficient to be fitted describing the etch rate reduction due to aspect ratio, and *W* is the width of the minimum etched spacing between the pillars. This model is intended as an approximation for etching rates and should closely approximate the rates seen for etching trenches of similar aspect ratios. The assumption made for this model is that the aspect ratio dependent etch rate scales linearly, the simplest possible model describing the aspect ratio effects. The etch depth verse time data points are plotted with the graphical solutions to the differential equation for the different pillar heights, presented in Fig. 2. *E* was

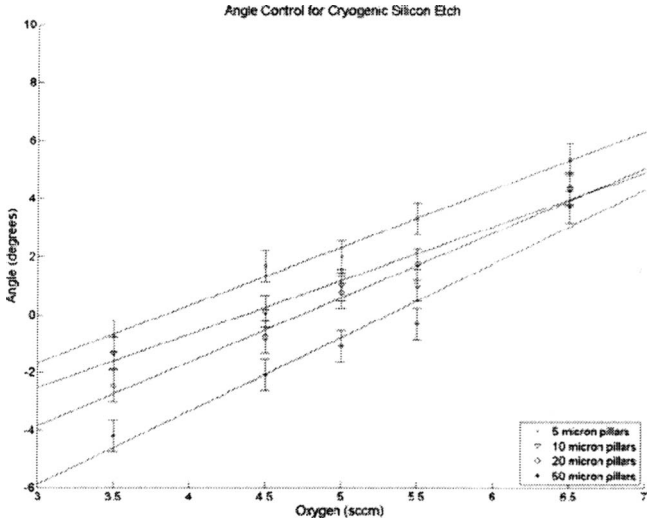

FIG. 3. Profile control of cryogenically etched silicon pillars. Error bars were placed to indicate sidewall angle variations due to temperature fluctuations of the substrate. Lines are linear fits to data intended to guide the eye.

determined to be 1.15 μm/min and b was 0.040 99 μm/min by curve fitting the width normalized data, D/w and t/w, resulting in an R-square fit of 0.9972,

$$D = \frac{E * w}{b} * (1 - e^{-b*t/w}). \quad (2)$$

The etch profile is easily controlled by either changing the temperature of the table or by changing the oxygen flow rate.[1] Altering either one of these conditions affects only the passivation rate with relatively good decoupling from the etching rate. However, we noted that temperature further controls notching at the top of pillars with high aspect ratios. Warmer temperatures produced notching which was round and smooth but pitted the surface of the pillar, whereas the colder temperatures produced notching which was squared and jagged. Optimization between these two conditions for the cryogenic etch was found to be −120 °C and profile control was then tuned using O_2 flow rates. By setting the O_2 to 3.5 SCCM (SCCM denotes cubic centimeter per minute at STP), the angle of the pillar sidewall was made slightly re-entrant, and by increasing the O_2 to 6.5 SCCM the pillar sidewall was made to taper positive, Fig. 3. A flow rate of 4.5 SCCM was determined to give approximately vertical sidewalls. Black silicon began to appear at 7.5 SCCM in the trenches between the pillars while still increasing the positive taper. The arrival of black silicon prevents further tuning for a positive taper, Fig. 4. For our system, the mass flow controller for the oxygen becomes unstable at flow rates of approximately 2 SCCM which prevents tuning the sidewall angle more in the re-entrant direction. These limitations combine to give about 7° of tunability across the different pillar widths. Similar pillars to those just described were then doped and used to study radial p-n junction solar cells.[5]

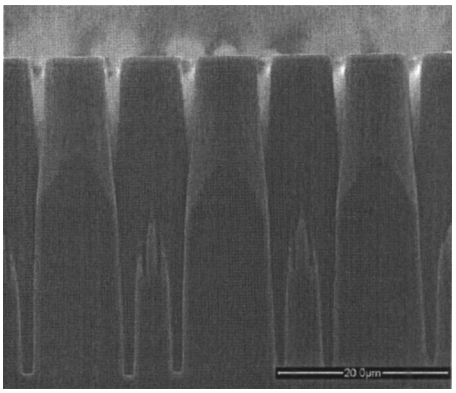

FIG. 4. Cross sectional SEM of 36 μm high, 5 μm diameter silicon pillars cryogenically etched with 7.5 SCCM of O_2 for an angle of 3.6°. Note the onset of black silicon between the pillars.

III. METAL LIFTOFF WITH PHOTORESIST: MAGNETIC SHIMS AND PLANAR MICROCOILS

Another positive advantage of the cryogenic silicon etch is the high selectivity of the etch rate of photoresist over silicon. This advantage can be utilized for improving metallization lift-off on silicon. Typically when lifting off a metallization layer using photoresist, care must be taken in obtaining resist sidewalls that are vertical or even slightly re-entrant, and the photoresist has to be substantially thicker than the deposited metal layer.[9] The approach which we describe here transfers the difficult lift-off profile requirements from the photoresist to the cryogenic silicon etch. As we demonstrated with the pillars, the sidewall profile is very easy to control and reproducible by optimizing etch parameters.[4,7,10] The high selectivity improves the relative height between the top of the photoresist to the silicon surface being metallized, thereby permitting thicker metal layers to be deposited. This enables creation of passive magnetic shims and electromagnetic coils by deposition of thick layers of iron and copper into silicon, Fig. 5. To the authors

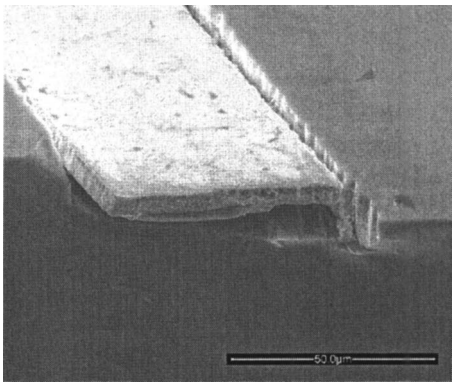

FIG. 5. Cross sectional SEM of a 6.5 μm thick evaporated iron ring in a 18.5 μm deep silicon trench. The 1.6 μm thick photoresist, used as the cryogenic etch mask, was also used for metal liftoff. This transferred the sidewall requirements for liftoff from the resist to the more controllable etch. Note that the pattern roughness along the edge of the trench was transferred from the mask to the silicon by the cryogenic etch.

TABLE II. Etch parameters for etching trenches for iron and copper coils in silicon.

Etch parameter	Units	Value	Etch parameter	Units	Value
SF_6	(SCCM)	90	ICP	(Watts)	1000
O_2	(SCCM)	6	RIE	(Watts)	3
Temperature	(Celsius)	−120	Pressure	(milliTorr)	10
Etch rate	(μm/min)	2.3	Helium	(Torr)	10

knowledge, this is the first time using the etch mask as also the metallization lift-off mask for deposition of thick metal or oxide layers on silicon.

With sample preparation similar to the previously mentioned approach, a 2 in. *p*-type silicon wafer was cryogenically etched to 18.5 μm depth to define patterns with various radii and widths, steps a and b in Fig. 6. Optimization for vertical sidewalls led to the following conditions (Table II).

Profilometer measurements taken before and after etching indicated photoresist losses only 0.2 μm, an approximate selectivity of 90:1. With over 1 μm of photoresist remaining, iron was thermally evaporated at a rate of 8 A/s to a final thickness of 6.5 μm, step d in Fig. 6. Lift-off was then performed using acetone, step e in Fig. 6. This created thick iron rings embedded in silicon, which was then placed on a 2 in. diameter NdFeB permanent magnet for passively shaping the magnetic field in nuclear magnetic resonance experiments.

This technique was also used in creating planar microcoil detectors in silicon,[11] Fig. 7. The previous etch recipe was applied to a 3 in., *p*-type, 1 mΩ cm silicon wafer to etch a four turn 750 μm radius microcoil. 1.5 μm of SiO_2 was then deposited in a plasma enhanced chemical vapor deposition reactor at 135 °C to provide electrical insulation between the copper wires being created and the silicon substrate, step c in Fig. 6. The insulating SiO_2 layer was followed by a 40 nm amorphous silicon deposition to improve metal adhesion. Prior to deposition, the center contact is mechanically fractured away to allow for copper to silicon Ohmic contacting and removing the need for a bridging contact, Fig. 8. Next, 10 μm of copper was thermally evaporated into the 20 μm deep trenches. Lift-off was again performed with acetone and a cotton swab. Due to the vertical profile of the etch and brittle nature of silicon dioxide precision shearing of the oxide can be seen at the top edge of the trench.

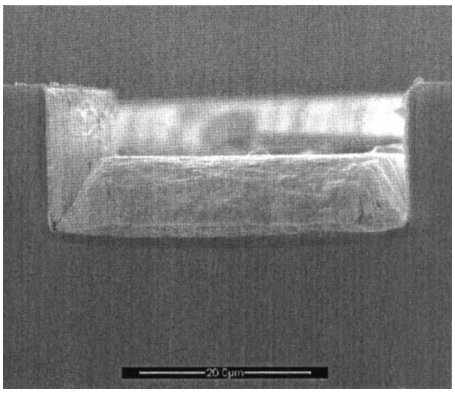

FIG. 7. Cross sectional SEM of 10 μm of evaporated copper in a 20 μm deep silicon trench insulated by 1.5 μm of SiO_2. The brightest material is the copper insulated by silicon dioxide, dark layer between the copper, and substrate.

IV. DEEP SILICON ETCHING USING TWO STEP PROCESSES MECHANICAL RESONATOR

Micromachining technology using silicon, MEMs, typically requires significant etch depths to be achieved, over 200 μm for the device described here. A widely used silicon etch to achieve this is the "Bosch" etch process which alternates an etching step with a passivation step.[12,13] While this etch allows for etch depths of several hundred microns to be achieved, it leaves "chopping" marks along the sidewalls

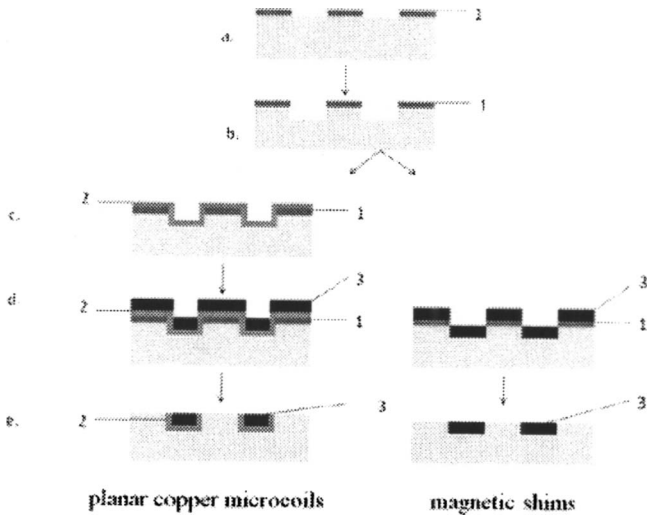

FIG. 6. Fabrication sequences for metallization in silicon: (a) 1.6 μm of photoresist is patterned on a silicon substrate, (b) silicon is cryogenically etched to depths of approximately 20 μm, (c) SiO_2 is deposited (microcoil sequence only), (d) thermal evaporation of thick layers of metal, and (e) lift-off using acetone.

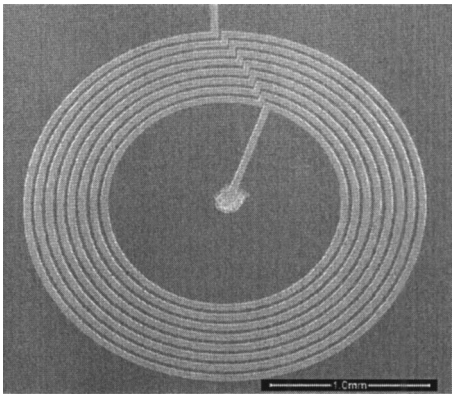

FIG. 8. SEM of a 750 μm radius planar microcoil fabricated in silicon using a single photolithography mask. The copper turns are imbedded into silicon cryogenically etched and metal lift-off is performed using the 1.5 μm thick etch mask. No bridging contact to center is needed as the current is sourced into the silicon substrate as an Ohmic contact at the center of the coil.

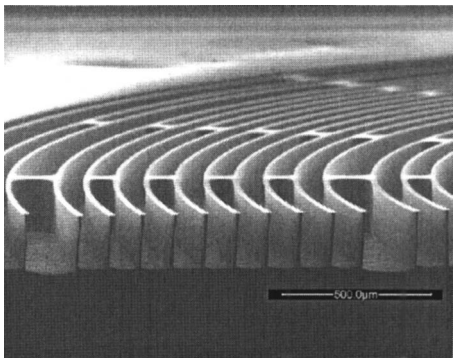

FIG. 9. SEM of a cross section of the MEM resonator etched using a two step cryogenic etch and a 5.5 μm thick silicon dioxide etch mask to a depth of 200 μm.

which are approximately several microns in size.[14] This marking can be detrimental when the device applications rely on interactions with the sidewalls such as the mechanical resonator fabricated here. Using the cryogenic etch for this application offers the elimination of the chopping marks. However, maximum etch depth for the cryogenic etch is ultimately mask erosion limited or aspect ratio limited, the later limitation becomes significant after several tens of micrometer depths as previously described.[15]

To improve the mask erosion quality either the forward power is reduced or a thicker mask may be employed. Hindering fabrication with thicker silicon dioxide masks is the slow growth or deposition rates required with the added difficulty of etching a pattern into silicon dioxide while hindering resists masks thicker than 1.5 μm are the problems of thermal gradients on the mask causing cracking. Increasing the RIE power imparts more momentum to the ions allowing for the gases to achieve greater depths, improving the aspect ratio limitation. However, since the milling action of the ions has increased, the selectivity of the mask is typically reduced and maximum depth attainable is subsequently reduced. Increasing the RIE power also requires an increase in passivation gas, oxygen, moving the etch into the black silicon regime, as demonstrated with the pillars.

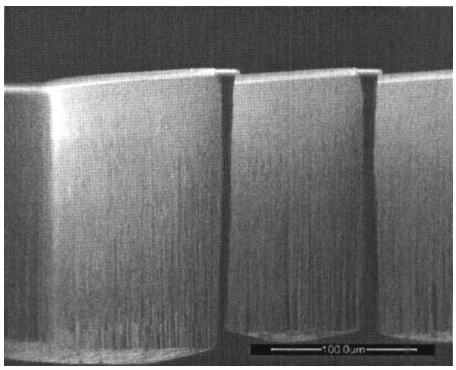

FIG. 10. SEM of a cross section of the MEM resonator's sidewalls etched using a two step cryogenic etch to a depth of 200 μm. Note that 3.5 μm of etch mask still remains.

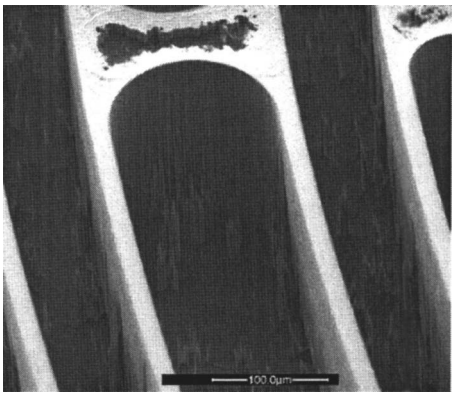

FIG. 11. SEM of a cross section imaged at an angle of 45° of the MEM resonator's sidewalls etched using only the second step of the two step etch in Table III. Note that the silicon dioxide mask has been eroded through after only achieving about 160 μm etch depth.

Combining two etches then enables optimization for the required depth. The first etch, using lower RIE power to etch as deep as possible, while minimizing damage to the etch mask, is followed by a second etch with higher RIE power. Thus deeper cryogenic etches can be achieved. This technique is used for creation of MEM mechanical resonators. The diameter of such a resonator is 7 mm, defined with a 5.5 μm thick silicon dioxide etch mask. Structures of the resonator rings are 20 μm wide ridges separated by 80 μm. The 80 μm separations are the etch trenches. This two step cryogenic etch achieves over 200 μm of depth, 2 μm of oxide mask loss, and with less than 3 μm of lateral etching or undercutting; a remarkable 1.5% ratio, Figs. 9 and 10. As a comparison, the second etch step was performed for 140 min using the same thickness oxide mask. The mask had eroded and began etching the silicon after only 160 μm of etch depth, Fig. 11.

To achieve the depth required for the resonator, the following two-step etch process is performed (Tables III and IV).

V. CONCLUSIONS

This work has demonstrated how the cryogenic ICP-RIE etch can be utilized to perform deep silicon etches for applications ranging from solar cell construction to the definition of liftoff-fabricated electromagnetic structures. With relatively little photoresist, 100 μm tall pillars can be constructed with smoother sidewalls than possible by using chopping etches such as the Bosch etch. We also describe the

TABLE III. Etch parameters for first step of MEM resonator etch in silicon.

Etch parameter	Units	Value	Etch parameter	Units	Value
SF_6	(SCCM)	90	ICP	(Watts)	900
O_2	(SCCM)	6	RIE	(Watts)	3
Temperature	(Celsius)	−140	Pressure	(milliTorr)	10
Etch rate	(μm/min)	1.3	Helium	(Torr)	10

TABLE IV. Etch parameters for second step of MEM resonator etch in silicon.

Etch parameter	Units	Value	Etch parameter	Units	Value
SF_6	(SCCM)	90	ICP	(Watts)	900
O_2	(SCCM)	6	RIE	(Watts)	15
Temperature	(Celsius)	−140	Pressure	(milliTorr)	10
Etch rate	(μm/min)	1.3	Helium	(Torr)	10

limits of the fabrication depths of cryoetched trenches and the control over the sidewalls of lift-off metallization. In this liftoff procedure, the fabrication requirements replace challenging photoresist chemistry to control sidewalls of thick polymer layers with the geometric control over the sidewalls and etch depth available from cryogenic silicon etching procedures. Cryogenic etching can also be utilized for deep silicon etching of MEMs mechanical resonator structures using a two step process. This allows for the etch to minimize the etch mask thickness requirements needed for deep reactive ion etching. Etch recipes to reproduce all these etches were also provided.

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